CLAIMS

What is claimed is:

1. A circuit for protecting the values stored in a BISR repair block, comprising:

a plurality of soft latches within the BISR repair block, the soft latches being coupled together to form a BISR scan chain for holding BISR repair information; and

means for providing a chip level scan enable signal for enabling a scan test and a scan hold control signal for controlling holding of the repair information in the soft latches of the BISR scan chain,

wherein the chip level scan enable signal and the scan hold control signal cooperate to control connection of the BISR scan chain to other scan chains during a scan test, so that the BISR repair information is held within the soft latches.

2. The circuit as claimed in claim 1, wherein the chip level scan enable signal and the scan hold control signal cooperate to prevent the BISR scan chain from being connected to other scan chains.

3. The circuit as claimed in claim 1, further comprising means for providing a diagnose enable signal, the diagnose enable signal cooperating with the chip level scan enable signal and the scan hold control signal for enabling debugging of logic connecting the BISR scan chains.

4. The circuit as claimed in claim 3, further comprising means for providing a BISR scan signal suitable for causing the scan test to be run.

5. The circuit as claimed in claim 4, wherein the chip level scan enable signal, the scan hold control signal, the diagnose enable signal and the BISR scan signal are combined to provide a test enable signal for controlling connection of the BISR scan chain to other scan

chains during a scan test.

6. The circuit as claimed in claim 5, wherein the test enable signal is determined by the expression

$$TE = BS \bullet \overline{DE} \bullet \overline{CLSE.} \bullet SHC + DE \bullet CLSE. \bullet SHC$$

wherein TE is the test enable signal, BS is the BISR scan signal, DE is the diagnose enable signal, CLSE is the chip level scan enable signal, and SHC is the scan hold control signal.

7. The circuit as claimed in claim 3, wherein the BISR scan chain is connected in a single scan chain separate from logic forming other scan chains, and wherein the BISR scan chain is activated when required.

8. The circuit as claimed in claim 3, wherein the BISR scan chain is multiplexed with a normal scan chain.

9. The circuit as claimed in claim 8, wherein when the diagnose enable signal is low the BISR scan chain is bypassed by the scan test and wherein when the diagnose enable signal is high, the BISR scan chain is put in the scan test path.

10. A method for protecting the values stored in a BISR repair block, comprising:
storing repair information in a plurality of soft latches within the BISR repair block, the soft latches being coupled together to form a BISR scan chain for holding the BISR repair information; and
providing a chip level scan enable signal for enabling a scan test and a scan hold control signal for controlling holding of the repair information in the soft latches of the BISR scan chain,
wherein the chip level scan enable signal and the scan hold control signal cooperate to control connection of the BISR scan chain to other scan chains during a scan test, so that the BISR repair information is held within the soft latches.

11. The method as claimed in claim 10, wherein the chip level scan enable signal and the scan hold control signal cooperate to prevent the BISR scan chain from being connected to other scan chains.

12. The method as claimed in claim 10, further comprising providing a diagnose enable signal, the diagnose enable signal cooperating with the chip level scan enable signal and the scan hold control signal for enabling debugging of logic connecting the BISR scan chains.

13. The method as claimed in claim 12, further comprising providing a BISR scan signal suitable for causing the scan test to be run.

14. The method as claimed in claim 13, wherein the chip level scan enable signal, the scan hold control signal, the diagnose enable signal and the BISR scan signal are combined to provide a test enable signal for controlling connection of the BISR scan chain to other scan chains during a scan test.

15. The method as claimed in claim 14, wherein the test enable signal is determined by the expression

$$TE = \overline{BS} \cdot \overline{DE \cdot CLSE.} \cdot SHC + DE \cdot CLSE. \cdot SHC$$

wherein TE is the test enable signal, BS is the BISR scan signal, DE is the diagnose enable signal, CLSE is the chip level scan enable signal, and SHC is the scan hold control signal.

16. The method as claimed in claim 15, wherein the scan hold control signal and the diagnose enable signal are provided by a TAP controller.

17. The circuit as claimed in claim 12, wherein the BISR scan chain is connected in a single scan chain separate from logic forming other scan chains, and wherein the BISR scan chain is activated when required.

18. The circuit as claimed in claim 12, wherein the BISR scan chain is multiplexed with a normal scan chain.

19. The circuit as claimed in claim 18, wherein when the diagnose enable signal is low the BISR scan chain is bypassed by the scan test and wherein when the diagnose enable signal is high, the BISR scan chain is put in the scan test path.

20. A memory employing a Built In Self Repair circuit, comprising:

a circuit for protecting the values stored in a BISR repair block, including:

an array of memory elements;

a BISR circuit for providing testing and soft repair of a memory element within the array;

a plurality of soft latches controlled by the BISR circuit, the soft latches being coupled together to form a BISR scan chain for holding BISR repair information; and

means for providing a chip level scan enable signal for enabling a scan test and a scan hold control signal for controlling holding of the repair information in the soft latches of the BISR scan chain,

wherein the chip level scan enable signal and the scan hold control signal cooperate to control connection of the BISR scan chain to other scan chains during a scan test, so that the BISR repair information is held within the soft latches.

21. The memory as claimed in claim 20, wherein the chip level scan enable signal and the scan hold control signal cooperate to prevent the BISR scan chain from be connected with other scan chains.

22. The memory as claimed in claim 20, further comprising means for providing a diagnose enable signal, the diagnose enable signal cooperating with the chip level scan enable signal and the scan hold control signal for enabling debugging of logic connecting the BISR scan chains.

23. The memory as claimed in claim 22, further comprising means for providing a BISR scan signal suitable for causing the scan test to be run.

24. The memory as claimed in claim 23, wherein the chip level scan enable signal, the scan hold control signal, the diagnose enable signal and the BISR scan signal are combined to provide a test enable signal for controlling connection of the BISR scan chain to other scan chains during a scan test.

25. The memory as claimed in claim 24, wherein the test enable signal may be determined by the expression

$$TE = BS \bullet \overline{DE} \bullet \overline{CLSE.} \bullet SHC + DE \bullet CLSE. \bullet SHC$$

wherein TE is the test enable signal, BS is the BISR scan signal, DE is the diagnose enable signal, CLSE is the chip level scan enable signal, and SHC is the scan hold control signal.

26. The circuit as claimed in claim 22, wherein the BISR scan chain is connected in a single scan chain separate from logic forming other scan chains, and wherein the BISR scan chain is activated when required.

27. The circuit as claimed in claim 22, wherein the BISR scan chain is multiplexed with a normal scan chain.

28. The circuit as claimed in claim 27, wherein when the diagnose enable signal is low the BISR scan chain is bypassed by the scan test and wherein when the diagnose enable signal is high, the BISR scan chain is put in the scan test path.